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InAs/InP Radial Nanowire Heterostructures as High Electron Mobility Devices

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ABSTRACT

Radial core/shell nanowires (NWs) represent an important class of one-dimensional (1D) systems with substantial potential for exploring fundamental materials electronic and photonic properties. Here, we report the rational design and synthesis of InAs/InP core/shell NW heterostructures with quantum-confined, high-mobility electron carriers. Transmission electron microscopy studies revealed single-crystal InAs cores with epitaxial InP shells 2–3 nm in thickness, and energy-dispersive X-ray spectroscopy analysis further confirmed the composition of the designed heterostructure. Room-temperature electrical measurements on InAs/InP NW field-effect transistors (NWFETs) showed significant improvement in the on-current and transconductance compared to InAs NWFETs fabricated in parallel, with a room-temperature electron mobility, 11 500 cm²/Vs, substantially higher than other synthesized 1D nanostructures. In addition, NWFET devices configured with integral high dielectric constant gate oxide and top-gate structure yielded scaled on-currents up to 3.2 mA/μm, which are larger than values reported for other n-channel FETs. The design and realization of high electron mobility InAs/InP NWs extends our toolbox of nanoscale building blocks and opens up opportunities for fundamental and applied studies of quantum coherent transport and high-speed, low-power nanoelectronic circuits.

Central to the "bottom-up" vision for nanoscale science and technology is the design and rational synthesis of building blocks with well-defined physical properties.[1] Semiconductor NWs represent a broad class of one-dimensional (1D) building blocks in which significant progress is being made in atomic to nanometer scale control of materials morphology, size, and composition,[1−4] including the growth of axial,[2] radial,[3] and branched[4] NW heterostructures. In the case of radial NW heterostructures,[3,5a−c] the controlled growth of one or more shells can passivate existing surface states, enable new interface properties, and introduce unique electronic and photonic function. For example, the energy band line-up at the Ge and Si interface of Ge/Si core/shell NWs[5] leads to the accumulation of high-mobility hole carriers, which have enabled fundamental studies of quantum transport [5a,b] and the realization of the highest performance p-channel NWFETs to date.[5c]

There has also been considerable effort placed on developing high electron mobility NWs with InAs, which has a small electron effective mass and correspondingly high bulk electron mobility,[6] the focus of a number of groups.[7] Reported electron mobilities for InAs NWs have been substantially lower than bulk values[7] and thus suggest that scattering processes in the NWs, including ionized impurity and surface scattering,[7d] reduce mobility. Hence, structures that passivate and/or protect the surface of InAs NWs might lead to enhanced transport properties. To this end, we report studies of InAs/InP core/shell NWs in which the InAs surfaces have been passivated with a nanometer-thick epitaxial InP conformal shell. Our design aims at creating a cylindrical quantum well populated with high-mobility electrons via a radial core/shell NW heterostructure motif. We chose InP as a shell material because the conduction band offset of ∼0.52 eV provides a good confinement potential for electrons (inset, Figure 1a) and because the type-I quantum well structure also confines holes that may be generated thermally or as a result of impact ionization in the channel.[8] From a structural perspective, the lattice mismatch between InAs and InP is relatively large, ∼3.1%, and places constraints on achieving defect-free NW structures necessary for realizing high carrier mobility. Theoretical[9] and experimental studies[10] of planar structures suggest a critical thickness of approximately 2−3 nm, and thus we expect that

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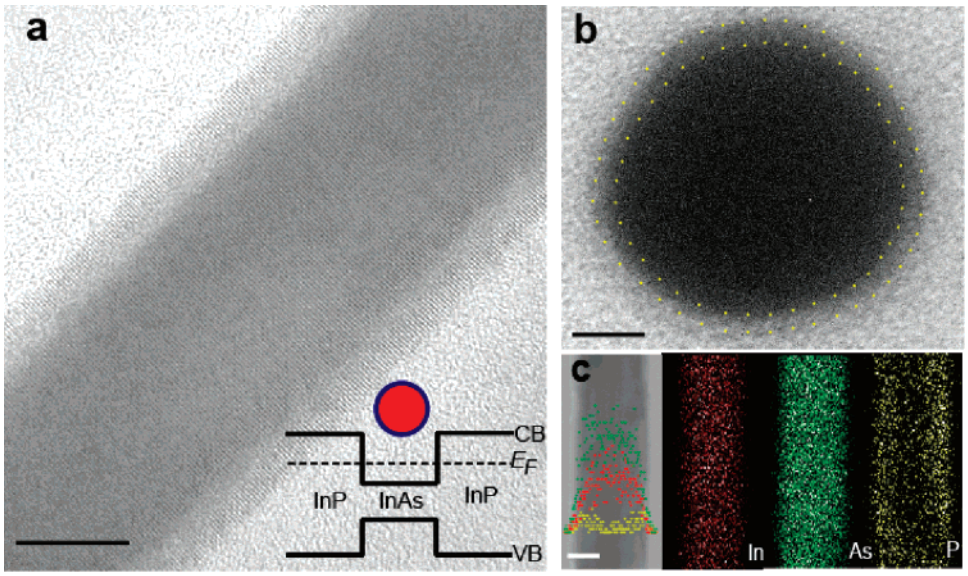

Figure 1. (a) HRTEM of a representative InAs/InP NW. Scale bar is 10 nm. Inset, cross-sectional schematic of an InAs/InP NW (red, InAs; blue, InP) and the corresponding band diagram. (b) Bright-field TEM image of an InAs/InP NW cross section. Dotted lines highlight the interfaces between layers. Scale bar is 5 nm. (c) Bright-field STEM image with cross-sectional EDX elemental line-scanning data (left) and the corresponding EDX elemental mapping of an InAs/InP NW. Scale bar is 10 nm.

InAs/InP core/shell NWs should remain structurally coherent when the shell thickness is near this value.

The InAs/InP core/shell NWs were prepared by a two-step synthetic methodology involving (i) Au nanoparticle catalyzed axial growth of the InAs NW core followed by (ii) radial growth of the InP shell. Clean, epitaxial growth of the InP shell was achieved using in situ source exchange and independent control of source and growth temperatures.[11] Representative high-resolution transmission electron microscopy (HRTEM) images of InAs/InP core/shell NWs (Figure 1a) show clearly contrast between InAs core and InP shell materials. The lattice-resolved images exhibit single-crystalline wurtzite structure with the growth along [001] direction. The InAs core in Figure 1a has a diameter of ~20 nm, while the InP shell has a thickness of ~2 nm. The interface between the core and shell is epitaxial and without visible dislocations, where a defect-free interface is important for achieving high electron mobility. Cross-sectional TEM images of InAs/InP NWs (Figure 1b)[12] further demonstrate that the InP shell is uniform around the entire InAs NW core. In addition, bright-field scanning transmission electron microscopy (STEM) images together with energy-dispersive X-ray (EDX) mapping (Figure 1c) confirms that the core/shell contrast observed in Figures 1a,b arises from the well-defined spatial distribution of As and P elements in the core and shell, respectively, of the NW structures.

The electrical transport properties of these new InAs/InP core/shell NWs were studied initially in a NWFET configuration with back-gate electrode.[13] Room-temperature current (I_{ds}) versus gate voltage (V_{gs}) data recorded on a representative InAs/InP NW device with a total diameter of 25 nm and channel length (L_g) of 2 μm (Figure 2a) features an on-current of ~7 μA and a peak transconductance (g_m) of ~2.2 μS, at a drain-source voltage of 0.1 V. For comparison, $I_{ds}-V_{gs}$ data were also recorded on InAs NW devices fabricated in parallel using NWs having the same diameter and channel length as the core/shell structures (Figure 2b). The homogeneous InAs NWFETs exhibit a relatively large positive threshold voltage of ~5 V, which indicates that there is a low level of ionized dopants in our core nanowires. We note that other reported InAs NWFETs[7] have shown a negative threshold voltage, which suggests substantial doping in the homogeneous NWs. Importantly, comparison of our InAs and InAs/InP devices demonstrates a shift in the threshold voltage toward $V_{gs} = 0$ and a substantial increase in on-current for the InAs/InP core/shell versus InAs NW structures. Significantly, the comparison of the g_m values show an approximately 5-fold increase for InAs/InP (2.2 μS) versus InAs (0.45 μS), which corresponds to a substantially enhanced electron mobility. All these transport features are consistent with the formation of a quantum confined electron gas in the InAs/InP core/shell radial NW heterostructures.

In addition to rational band structure design, we believe that the high-quality InAs NW cores synthesized in these studies are also important to achieving high-performance devices. Logarithmic scale plots of $I_{ds}-V_{gs}$ curves for both InAs and InAs/InP NW devices (Figure 2a,b, green lines) exhibit off-current <0.2 nA and subthreshold slopes (S) < 1 V/decade. Most reported InAs NW devices have shown much larger off-currents (>1 μA) and poor subthreshold behavior (S > 3 V/decade), possibly due to the incorporation of dopants and/or vacancies during growth.[7a-c] Our ability to optimize InAs NW cores independently of the InP shell growth was critical to realizing this behavior in our studies, and we believe further efforts in this direction (i.e., improving the InAs NW purity) could yield additional improvements in the device properties.

Temperature-dependent electrical transport measurements were carried out to further characterize the InAs/InP NWs. Conductance (G) vs V_{gs} data (Figure 3a) show that the on-

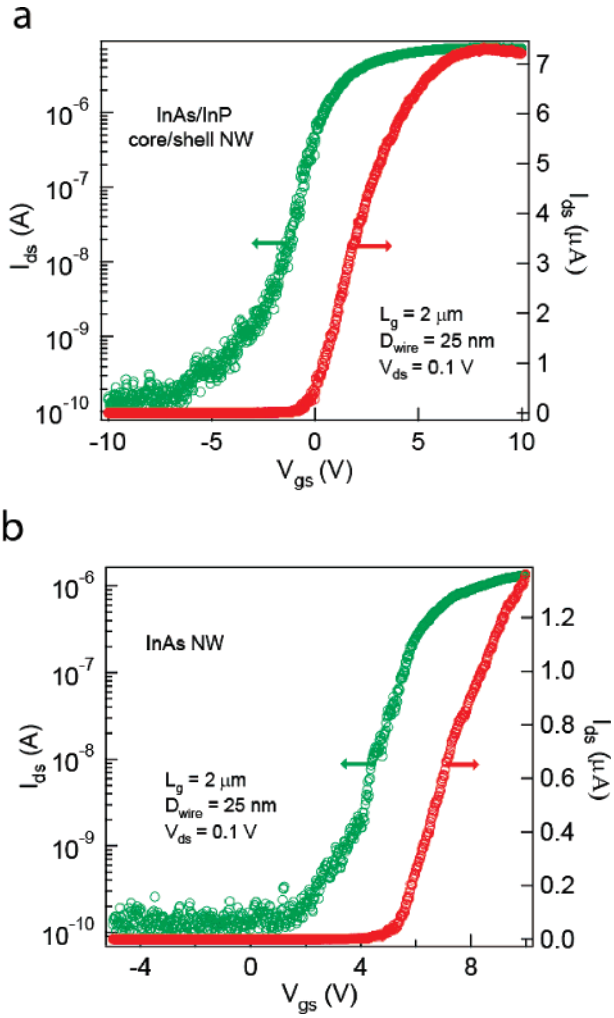

Figure 2. (a) $I_{ds}-V_{gs}$ data for a 25 nm diameter InAs/InP NW back-gated FET with $L_g = 2$ μm at $V_{ds} = 0.1$ V, plotted on linear (red) and logarithmic (green) scales. (b) $I_{ds}-V_{gs}$ data for a 25 nm diameter InAs NW back-gated FET fabricated in parallel with same channel length, plotted on linear (red) and logarithmic (green) scales.

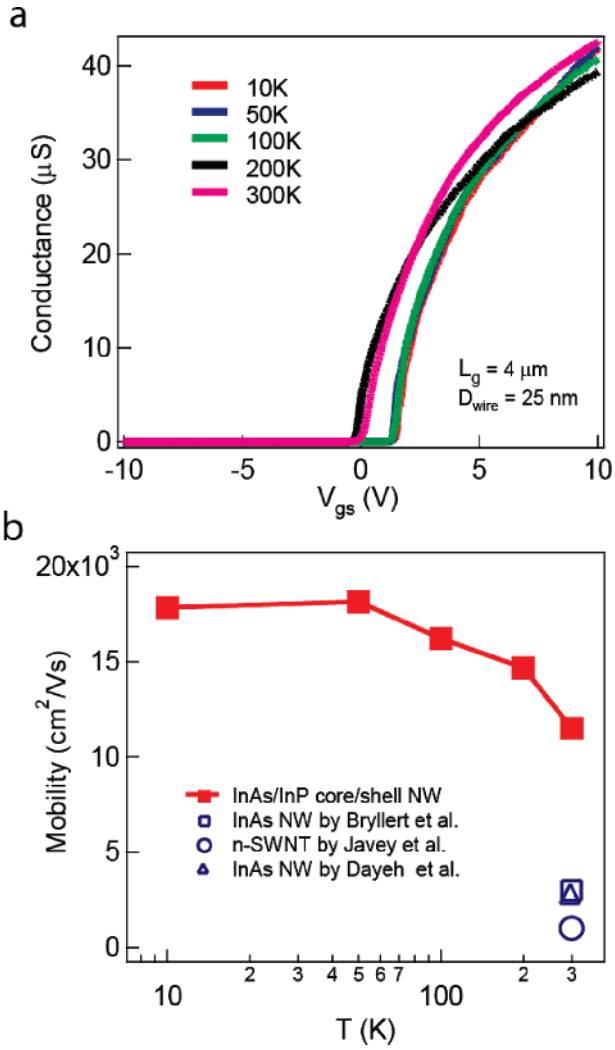

Figure 3. (a) $G-V_{gs}$ data measured at temperatures from 300 to 10 K for a 25 nm diameter InAs/InP back-gated NWFET with $L_g = 4$ μm. (b) Calculated electron mobility of the InAs/InP NW at different temperatures.[16] For comparison, the highest room-temperature electron mobility values reported in other 1D nanostructures are also included.

state conductance, ca. 40 μS, changes little as temperature decreases. This fact implies that the number of 1D subbands participating in transport does not vary with decreasing the temperature. We also find that the threshold voltage exhibits a small shift for $T > 100$ K. This shift may reflect a freeze-out of surface states[14] and would be consistent with the larger than theoretical value of S discussed above. The temperature-dependence of the field-effect electron mobility (Figure 3b), which was calculated using the charge control model,[15,16] shows that the electron mobility of the InAs/InP NW devices increases from 11 500 cm^2/Vs at room temperature and then saturates at 18 000 cm^2/Vs for $T < 100$ K. It is worth mentioning that contact resistance was not taken into account in our mobility values and thus that higher mobility values could be achieved by subtracting this series resistance term and/or optimization of contact transparency.

The temperature-dependent mobility results obtained for our InAs/InP core/shell NWs are distinct from those commonly observed in uniformly doped III−V materials,[17] which show carrier freeze-out and dramatically lower mobility for $T < 100$ K but similar to two-dimensional electron gas (2DEG) systems studied extensively using planar heterostructures.[17] These comparisons provide evidence for 1DEG formation in the InAs/InP NW heterostructures. We also note that core/shell NW electron mobility shows a weaker temperature dependence before saturation than classical 2DEGs.[16] This fact indicates that (i) ionized impurity and interface scattering, which dominate in the low-temperature regime, may limit electron mobility in our devices and (ii) phonon scattering has been substantially suppressed in our 1D structures.[18] Future work focused on improving the purity of the InAs NW core and epitaxial shell growth should help to address better the origins of these differences with 2DEG results.

Our data can also be compared to recent electron mobility values reported in other n-channel NW and carbon nanotube devices (Figure 3b). Bryllert et al. reported an electron mobility of ~3000 cm^2/Vs in vertical InAs NW transistors with novel cylindrical gate structure,[7a] while Dayeh et al. reported a similar value of ~2740 cm^2/Vs in back-gated InAs

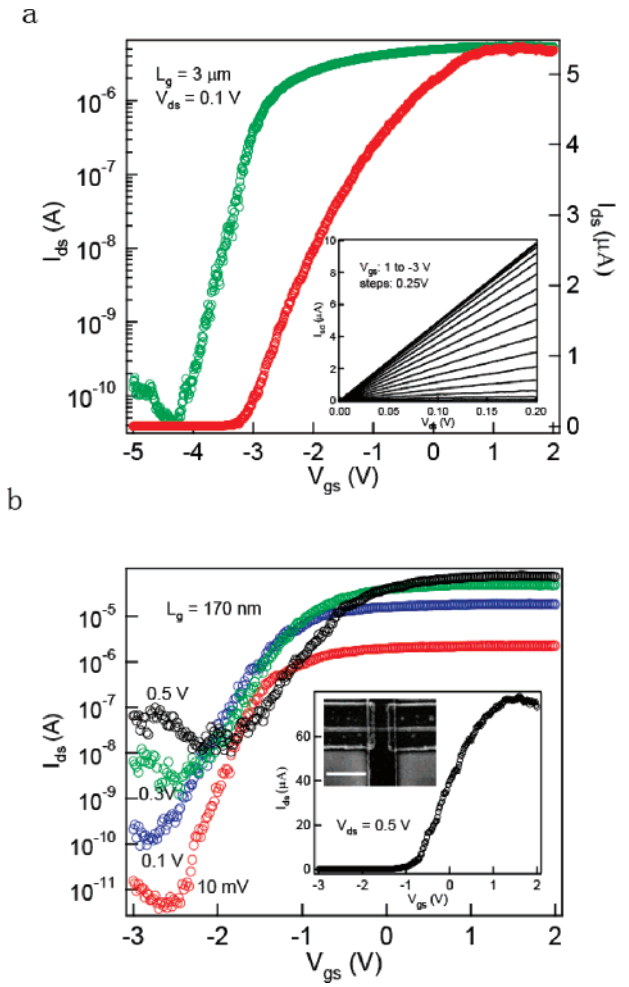

Figure 4. (a) $I_{ds}-V_{gs}$ data for a 25 nm diameter InAs/InP nanowire top-gate FET with $L_g = 3$ μm at $V_{ds} = 0.1$ V, plotted on linear (red, right) and logarithmic (green, left) scales. Inset: $I_{ds}-V_{ds}$ data recorded at V_{gs} values from +1.0 to −3.0 V in steps of 0.25 V. (b) $I_{ds}-V_{gs}$ data for a 25 nm diameter InAs/InP NW top-gated FET with $L_g = 170$ nm, in which red, blue, green, and black data points correspond to V_{ds} values of 0.01, 0.1, 0.3, and 0.5 V, respectively. Inset: linear scale plot of I_{ds} versus V_{gs} measured at $V_{ds} = 0.5$ V with top-view SEM image of the device. Scale bar is 500 nm.

NWFETs.[7c,19] The highest electron mobility in carbon nanotubes (CNTs) is ~1000 cm^2/Vs.[20] The 11 500 cm^2/Vs room-temperature electron mobility in our InAs/InP NW heterostructures, which represents a lower-bound value without contact resistance correction, is significantly higher than reported electron mobility data for these other 1D nanostructures and thus further substantiates the promise of the our radial core/shell approach for creating unique nanoscale building blocks.

NWFET devices with a top metal gated structure incorporating high-κ dielectric were fabricated to explore the potential of our InAs/InP NWs as high-performance FETs.[21] Typical $I_{ds}-V_{ds}$ curves (Figure 4a, inset) are linear at all measured gate voltages, indicating that the contacts are ohmic in our devices. These data also show that I_{ds} increases as V_{gs} increases from −3 to 1 V and thus that the device functions as an n-channel depletion-mode FET. The $I_{ds}-V_{gs}$ transfer curve recorded at $V_{ds} = 0.1$ V (Figure 4a) exhibits a peak transconductance g_m of ~3.0 μS and a subthreshold slope S of ~180 mV/decade for this $L_g = 3$ μm device. Both values are substantially better than achieved with comparable back-gate devices (Figure 2).

We have also fabricated shorter channel length InAs/InP NWFET devices to investigate scaling of critical device properties. Representative $I_{ds}-V_{gs}$ curves recorded at different V_{ds} obtained from an $L_g = 170$ nm device (Figure 4b) show an on−off ratio (>10^5) and S ~80 mV/decade for $V_{ds} = 10$ mV; these values decreased/increased to 10^3/260 mV/decade as V_{ds} increased to 0.5 V. This trend indicates a non-negligible short-channel effect in our device.[22] In addition, the maximum $I_{on} = 79$ μA and $g_m = 63$ μS (inset, Figure 4b) yield scaled[5c] values of I_{on}, 3.2 mA/μm, and g_m, 2.5 mS/μm, that are substantially higher than other NW and nanotube FETs[5c,20b,23] or n-channel MOSFETs.[24] A comparison of key parameters obtained for our InAs/InP core/shell and other high-performance FETs are summarized in Table 1. Notably, the scaled I_{on} value (38 mA/μm) exceeds substantially other systems and demonstrates the potential of InAs/InP NWFETs, assuming that short-channel effects can be overcome via improved device structure design.[24,25]

In summary, we have designed and synthesized single-crystal InAs/InP core/shell NW heterostructures with quantum-confined, high-mobility electron carriers. Transmission electron microscopy studies revealed single-crystal InAs cores with epitaxial InP shells 2−3 nm in thickness, and energy-dispersive X-ray spectroscopy analysis further confirmed the composition of the designed heterostructure. Systematic transport studies confirmed the core/shell NW band-structure design, demonstrated significant improvement of the on-current and transconductance compared to InAs NWFETs,

Table 1. Main FET Characteristics of Our InAs/InP Device and Those Reported in Other 1D Nanostructures and Planar CMOS

	InAs/InP NW	n-carbon nanotube (moderate doping)	n-carbon nanotube (high doping)	GaN/AlN/AlGaN NW	Ge/Si p-NW	planar CMOS
gate length (nm)	170	80	80	1000	190	35
V_{ds} (V)	0.5	0.5	0.5	1.5	1.0	1.2
I_{on} (mA/μm)	3.2	0.3	2.0	0.5	2.1	1.75
converted I_{on} (mA/μm)[a]	38	1.7	11	11	14	1.75
on/off ratio	10^3	10^4	10^2	10^7	10^3	10^4
subthreshold slope (mV/decade)	260	70	300	68	100	150

[a] For direct comparison, we calculated the converted I_{on} value by scaling to the drive voltage (1.2 V) and dimensions ($L_g = 35$ nm) of a state-of-the-art MOSFET (column 7), assuming (i) I_{on} is proportional to V_{sd}, (ii) the contact resistance is much smaller than the channel resistance, and (iii) the resistance of channel is proportional to length.

and yielded the highest electron mobility value to date, 11 500 cm^2/Vs at room temperature, for 1D nanoscale building blocks. In addition, NWFET devices configured with integral high dielectric constant gate oxide and metal top-gate structure yielded scaled on-currents up to 3.2 mA/μm, which are larger than values reported for other n-channel FETs. The design and realization of high electron mobility InAs/InP NWs extends our toolbox of nanoscale building blocks and could open up opportunities for fundamental and applied studies of quantum coherent transport and high-speed, low-power nanoelectronic circuits.

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Note Added after ASAP Publication. There was an error in the equation in ref 16 that appeared in the version published ASAP September 15, 2007; the corrected version was published ASAP September 17, 2007.

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